SECTION I. (AMENDMENTS TO THE CLAIMS)

A listing of claims 1-20 of the present application, which are amended herein with markings to show changes made, is provided below:

1-14. (Cancelled).

15. (Currently amended) A semiconductor structure comprising

a semiconductor substrate having at least one trench isolation region located therein, said at least one trench isolation region having sidewalls that extend to a common bottom wall;

a nitride liner present at least on portions of the sidewalls of the at least one trench isolation region, said nitride liner extends into the semiconductor substrate that surrounds the at least one trench isolation region and protects the sidewalls of the at least one trench isolation region so as to reduce stress in the semiconductor substrate, and

a trench dielectric material filling the at least one trench isolation region, wherein said trench dielectric material ~~is selected from the group consisting of~~ comprises SiO_2, tetraethylorthosilicate (TEOS), or ~~and~~ a high-density plasma oxide~~, and wherein said trench dielectric material comprises~~ with nitrogen species therein.

16. (Original) The semiconductor structure of Claim 15 wherein the nitride liner is present on the entire sidewalls and bottom wall of the at least one trench.

17. (Previously presented) A semiconductor structure comprising:

a semiconductor substrate having at least one trench isolation region located therein, said at least one trench isolation region having sidewalls that extend to a common bottom wall; and

a nitride liner present at least on portions of the sidewalls of the at least one trench isolation region, said nitride liner extends into the semiconductor substrate that surrounds the at least one trench isolation region and protects the sidewalls of the at least one trench

isolation region so as to reduce stress in the semiconductor substrate, wherein the nitride liner is a nitrided surface layer that has a thickness of about 0.1 to about 2.0 nm.

18. (Original) The semiconductor structure of Claim 15 further comprising NFET device regions and PFET device regions.

19. (Original) The semiconductor structure of Claim 18 wherein the trenches adjoining the NFETs contain the nitride liner on the entire sidewalls and bottom wall of each trench.

20. (Original) The semiconductor structure of Claim 18 wherein the sidewalls of the trenches adjoining the PFETs are void of any nitride liner.